Space Dynamics LABORATORY
Utah State University Research Foundation
1695 North Research Park Way, Logan, Utah 84341

REPORT TITLE			DOCUMENT NUMBER
WISE Digital Electronics Box Data Processing Description			SDL/06-070
PREPARED BY	**DATE**	**APPROVED BY**	**DATE**
Matthew Stites	1/28/06	Scott Schick	2-16-06
DISTRIBUTION			
JPL			

1. INTRODUCTION

This document describes the operation of the WISE digital electronics box (DEB) data processing firmware. It defines the various modes of firmware operation and the algorithm for generating output data. It outlines the conditions under which data is flagged as questionable. It also includes an analysis of the data path to show that a sufficient number of guard bits have been allocated to prevent overflow.

2. DESCRIPTION OF OPERATION

2.1 FUNCTIONAL OVERVIEW

The DEB includes four data processing boards, one dedicated to each band of focal plane data. Each board has one FPGA containing the data processing firmware. The same firmware is used in all four FPGAs. The functions of the firmware are to read focal plane data from a FIFO, perform the sample-up-the-ramp processing—storing intermediate data as necessary—and transmit processed data to a spacecraft interface board, which is also in the DEB. The firmware is also capable of performing a binning operation, which is described below. Binning is enabled via the installation of a hardware jumper on the data processing board.

2.2 CONFIGURABLE PARAMETERS

The data processing firmware includes a backplane interface that allows certain parameters to be updated through 1553 transactions. Any of these parameters can be updated at any point during the processing, but the updates will not take effect until the beginning of the next ramp. The three parameters that can be updated in this manner are

- saturation threshold value
- nine sample-up-the-ramp multiplication coefficients
- number of bits to be truncated from the output data

Each of these parameters is discussed in more detail below. One parameter that is not configurable on the data processing boards is the number of samples performed during a ramp. This is configured on the timing generation board which, in turn, controls the data processing boards. So, while the number of samples performed is critical in defining the output of the data processing firmware, it is not configured on the data processing board itself.

2.3 SAMPLE-UP-THE-RAMP

Digital pixel data are written into a FIFO on the data processing boards by the focal plane electronics. The FIFO is subsequently read by the data processing firmware and sample-up-the-ramp processing is performed. This processing is a simple multiply-accumulate operation. For the first read of the focal plane array every pixel value is multiplied by a single processing coefficient and 128 is added to the result. That value is then stored in RAM. For every subsequent read of the focal plane array all of the pixel values are multiplied by a coefficient specific to that read and added to the previous accumulated value which is retrieved from RAM. The resulting sum is then written back into the RAM, overwriting the previous sum. The mathematical formula for this processing is

$$d_m = 128 + \sum_{n=1}^{N} c_n p_{n,m} ,$$

where d_m is the output sum, N is the number of samples up the ramp, c_n are the multiplication coefficients, and $p_{n,m}$ are the pixel values. The n subscript defines the sample index and the m subscript defines the pixel index—there are 1024^2 pixels in an array. The number of samples up the ramp is a four-bit, unsigned value stored on the timing generation board. The default number of samples is 9. It can range from 0 to 15, but for typical operation should only range from 1 to 9, because the data processing firmware has storage for only nine multiplication coefficients. Each multiplication coefficient is a 5-bit, signed value, stored in sign-magnitude format. Thus, the coefficient values can range from -15 to +15 in integer steps. The default values for the processing coefficients are {-4, -3, -2, -1, 0, 1, 2, 3, 4}.

Once N reads of the focal plane array have been completed and the sample-up-the-ramp processing has completed, the resulting pixels must be scaled to a 15-bit value. This is done by truncating r least significant bits (LSBs) from the final sum and transmitting the next 15 bits to a spacecraft interface board. The truncation value r is a two-bit number that is forced to be one, two, or three. The default value is two.

It should be noted that all of the processing described above is done in the order the data is received from the focal plane electronics. The data processing does not change the order of the pixel stream. The pixels are transmitted to the spacecraft in the same order that the focal plane electronics wrote them into the data processing FIFO.

2.4 BINNING

The binning operation, if enabled, is performed after the sample-up-the-ramp processing is completed, but prior to the output truncation described above. Binning is performed on the sample-up-the-ramp output data, not on the input pixel data from the focal planes. The binning operation consists of adding four adjacent pixels (in a square pattern) and truncating the two least significant bits from the result. The resulting frame contains 262,144 pixels rather than the 1,048,576 pixels contained in a non-binned frame.

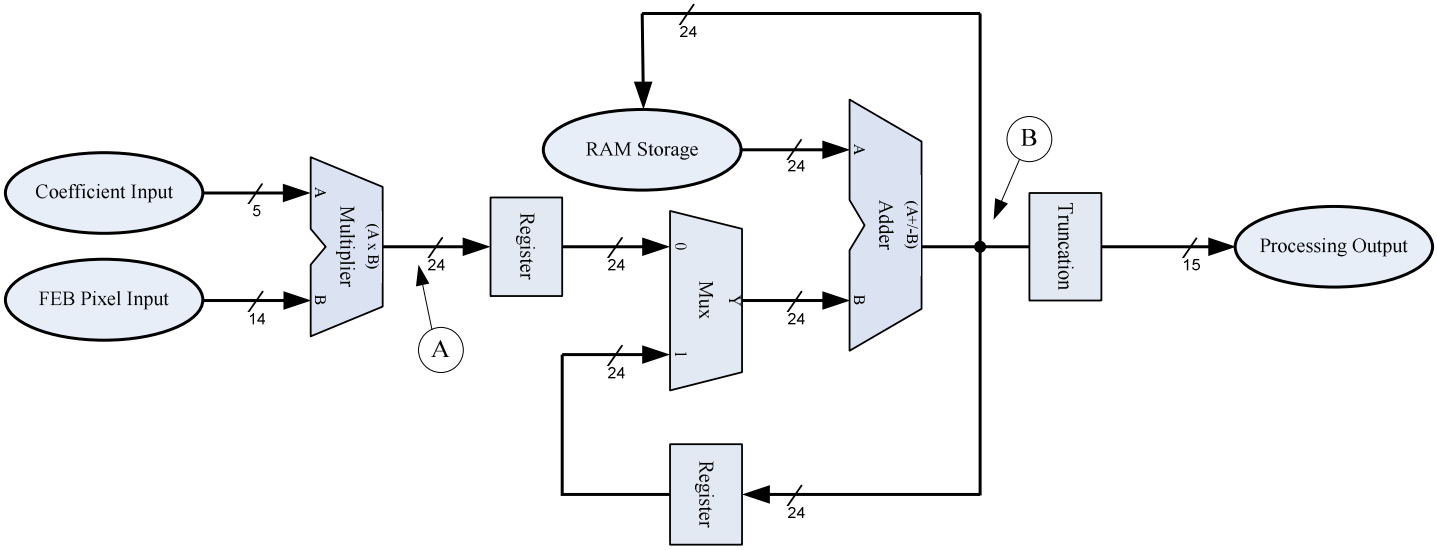
2.5 FLAG CONDITIONS

Data are flagged as suspect under either of two conditions: saturation detection and negative result. If an input pixel exceeds the saturation threshold value the intermediate sample-up-the-ramp sum is replaced with a marker to indicate the sample during which the pixel saturated. When the sample-up-the-ramp processing is completed and the resulting frame is transmitted to the spacecraft interface board, any pixel marked as saturated will be transmitted as 32,752 + n, where n is the sample number during which saturation was first detected. This result is equivalent to the hexadecimal value 7FFn. When binning is enabled, if any one of the four pixels to be added is marked as saturated, the output will be flagged as saturated. In this case, the output will be 32,752 + n, where n is the sample number during which saturation was first detected for any of the four pixels to be binned.

Because the values transmitted from the data processing firmware to the spacecraft interface boards are unsigned, there is no way to represent negative results. Therefore, if any sample-up-the-ramp result is negative the output to the spacecraft is replaced with 32,767 (7FFF hex). The 128 added at the beginning of the sample-up-the-ramp processing is intended to prevent negative values from resulting where the signal-to-noise ratio is very small. Thus, under normal operating conditions a negative value is unexpected and would be an indication of a "broken" pixel in the focal plane array.

3. DATA PATH ANALYSIS

An analysis is performed here to determine whether or not the potential for data overflow exists in the data processing firmware. The data processing data path is fairly simple and is shown below. All operations and data storage are performed using a sign-magnitude integer format. The only exceptions are the focal plane electronics box (FEB) pixel input and the processing output—both of which are positive, unsigned values. By using a sign-magnitude format overflow potential is determined only by the magnitude of a result and not by the sign of a result as a bit is always dedicated to the sign.



Registers and multiplexers do not perform operations that would lead to overflow, so long as their output bus is as wide as their input bus. This leaves only two locations which would be candidates for data overflow, labeled in the figure above as A and B. The maximum magnitude of an input coefficient is 15. The maximum value of an input pixel is 16,383. Therefore the maximum magnitude of product of the two is 245,745, which can be represented by 18 bits. Therefore, there is no potential for overflow at point A in the data path.

Analysis of point B in the data path requires an understanding of the sample-up-the-ramp processing and binning operations as described above. The upper branch at point B is used to store intermediate sample-up-the-ramp values while the lower branch is used in binning. For the intermediate sample-up-the-ramp values—upper branch—the worst-case scenario would have all of the coefficients equal to 15 and every input pixel equal to 16,383. For nine samples up the ramp this would lead to a final result of

$$d_m = 128 + \sum_{n=1}^{9} 15 \cdot 16{,}3863 = 2{,}211{,}833\,,$$

which can be represented as a 22-bit number. Therefore, there is no chance for the intermediate sample-up-the-ramp values to overflow. The worst-case scenario during binning—lower branch—would be for all four pixels

to be equal to the previous maximum value. This would give a result of 2,211,833·4 = 8,847,332 which would require a 24-bit magnitude when only 23 bits are available. This reflects an overflow condition. Overflow would be avoided if the result of the binning could be represented as a 23-bit magnitude. The maximum value in that case would be 7FFFFF hex or 8,388,607. Subtracting 128 and dividing this number by four gives a result of 2,097119.75. Dividing again by nine yields 233,013.31. As long as the average coefficient-pixel product is less than 233,013, overflow would be avoided. Assuming all multiplication coefficients were equal to 15, this would yield an average input pixel value of 15,534. These coefficient-pixel combinations are extremely unlikely. To guarantee overflow is never an issue multiplication coefficients should be selected carefully and/or a saturation threshold should be set so pixel values that would typically cause overflow instead generate a saturation marker.

Besides overflow, the truncation of the most-significant bits of the processing result to obtain a 15-bit output can also lead to a loss of data. The 24-bit data path analyzed above is only used for processing intermediate data. If the final result is larger than an 18-bit number (because up to three least-significant bits can be truncated), data will be lost. As with the overflow condition, multiplication coefficients, saturation thresholds, and the bit-truncation count need to be carefully chosen to avoid loss of data.

It is worth pointing out that when a similar worst-case analysis is repeated for the nominal multiplication coefficients shown above the maximum magnitude at point B in the data path—including binning—is 655,320 which can be represented as a 20-bit number. If binning is neglected, the maximum magnitude is an 18-bit number. Therefore there is no chance for overflow given the default configuration parameters and the chance of data loss due to MSB truncation is very small.

4. SUMMARY

The data processing firmware is designed to perform sample-up-the-ramp processing and binning and to flag potentially erroneous data. A handful of configurable parameters are made available to control this processing. The algorithms for generating the output data have been described above. As long as these algorithms are well understood and care is taken to configure the data processing firmware appropriately, any undesirable loss of data due to overflow or MSB truncation can be avoided.